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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/578,440	05/25/2000	Hajime Washio	49855(904)	6115

7590 05/07/2002

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EXAMINER	
ABDULSELAM, ABBAS L	
ART UNIT	**PAPER NUMBER**
2674	6

DATE MAILED: 05/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/578,440	Applicant(s) Washio et al.
	Examiner Abbas Abdulselam	Group Art Unit 2674

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-21 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-21 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3, 5

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. A copy of foreign document has been received.

Claim Rejections 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriyama et al. (USPN 6232945) in view of Ishii (USPN 6081131).

Regarding claims 1, 16 and 20, Moriyama teaches a shift register circuit containing multiple cascade-connected flip flops in synchronization with clock signals. See col. 2, lines 40-50. Moriyama teaches a display panel section (281) including multiple pixels arranged in a matrix form. Moriyama teaches scanning line driving circuit (293) with multiple scanning lines (Y1, Y2..Yn) and video signal line driving circuit (291) with multiple video signal lines. See Fig 1. Moriyama also teaches that the scanning line driving circuit in terms of voltage application at different timing (tsub0, tsub 1..tsub 4). See Fig 3 and col. 8, lines 12-53. Furthermore, Moriyama teaches the video signal line driving circuit that includes video signal selecting circuit (205) which outputs video signals data including non-displayed data. See col. 6, lines 32-43, col. 7, lines 54-59, 65-67, col. 8, lines 1-2 and Fig 2. Moreover, Moriyama teaches the video signal driving circuit in terms of matrix wiring section (201) and logic circuit (202) that will enable the display data to

be displayed on the pixels arranged on the (N-1)the line from the display area (502). See col. 8, lines 12-28 and Fig (1- 4). However, Moriyama does not teach about a level shifter for applying a clock signal and for increasing a voltage of a clock signal. On the other hand Ishii teaches a Liquid crystal device including level shifters (51, 52, 53, 54). See Fig 8. Ishii also teaches a logic amplitude level converter (10) including a voltage biasing means. See Fig 3, col. lines 44-50.

Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify Moriyama's display device to include Ishii's level shifters. One would have been motivated in view of the suggestion in Ishii that the level shifters can be used for desired application and increment of clock signals. The use of level shifters helps Liquid crystal device function more effectively as taught by Ishii.

Regarding claims 2-3, Moriyama teaches that when a pulse is inputted to the flip flop 22 sub1 from outside, the start pulse is transferred to the succeeding stage flip-flop 22 sub 2. See col. 15, lines 10-16.

Regarding claims 4-5 and 21, Moriyama teaches a reset circuit for outputting a signal for selecting the scanning line based on the output of the flip-flop of the shift register. See col. 3, lines col. 3, lines 39-43.

Regarding claim 6, Moriyama teaches the input stage switching circuit (23) in terms of multiple flip-flops as well as pulse input and output. See col. 15, lines 7-18.

Regarding claims 7-9 and 11-12, Ishii teaches a level shifter (2) obtaining an output clock signal, V (out) through selector /offset circuits (1A, !B). See col. 1, lines 30-42 and Fig 11.

Regarding claim 10, Ishii teaches a level shifter (2) in terms of constant current source (4). See Fig 11.

Regarding claim 13, Ishii teaches an output inverter (3) of an output-stage buffer circuit for buffering interactions in the input-output process. See col. 1, lines 40-43.

Regarding claim 14, Ishii teaches a level shifter (53) with respect to horizontal clock signals (HCK1, HCK2). See Fig 8.

Regarding claim 15, Moriyama teaches a display device with 853 times 480 pixels. See Fig 14. Moriyama also teaches the input staging circuit (23) as it relates to the output of the flip flop 22 sub 107. See col. 15, lines 17-18.

Regarding claims 17-19, Moriyama teaches a display device as shown in Figure 1. See (293, 100, 121, 351) of Fig 1.

Conclusion

3. The prior art made of record and not relied upon is considered to applicant's disclosure. The following arts are cited for further reference.

U.S. Pat No. 5,642,128 to Inoue

U.S. Pat No. 6,160,533 to Tamasi et al.

U.S. Pat No. 6,219,020 to Furuhashi et al.

U.S. Pat No. 6,271,818 to Yamazaki et al.

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to crustal park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Abbas Abdulselam

Examiner

Art Unit 2674